NOVEMBER/DECEMBER 2024

CEEL62B/BEEL62B — DIGITAL SYSTEM DESIGN

Time : Three hours Maximum : 75 marks

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SECTION A — (10 × 2 = 20 marks)

Answer ALL questions.

1. Define binary codes and list out the different codes.
2. Draw the 2D representation of K-map for 3 variables.
3. What is a meant by combinational Analysis?
4. Define Hardware Description Language.
5. Define active low outputs or state.
6. Define the term PLD.
7. Define state reduction.
8. What is meant by asynchronous and synchronous counters?
9. Define flow table.
10. What is meant by race condition?

SECTION B — (5 × 5 = 25 marks)

Answer ALL questions.

11. (a) Write a number $(123)_{10}$ in binary and BCD.

Or

(b) Short note on gray code.

12. (a) Draw the combinational logic circuit for A'B + AB + C'.

Or

(b) Explain the half subtractor circuit and truth table with suitable logical figure.

13. (a) Explain in detail PLA arrangement.

Or

(b) Differentiate PLA and PAL.

14. (a) Explain the working function of SR flip flop.

Or

(b) Discuss any one of the counter with suitable logic diagram and function table.

15. (a) Give a short note on reduction of state tables.

Or

(b) Brief account on hazards in sequential circuit.

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SECTION C — (3 × 10 = 30 marks)

Answer any THREE questions.

16. Show that A'B + B'C + C'A = .AB' + BC' + CA'.

17. Discuss the full subtractor circuit and truth table with suitable logical figure.

18. Explain the working function of Multiplxer in detail.

19. Explain the working function shift register with suitable logic design for SISO and SIPO.

20. Discuss in analysis and design of asynchronous sequential circuits.

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